UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,890	07/20/2005	Philippe Robert	124102	4335

25944 7590 01/12/2009

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
CULBERT, ROBERTS P	
ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
01/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,890	ROBERT ET AL.	
	Examiner	Art Unit	
	Roberts P. Culbert	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 11/26/08 have been fully considered.

Applicant has argued that the references fail to teach "the embedding layer surrounding the sacrificial layer, an interface being formed between the sidewalls of the sacrificial layer and internal sidewalls of the embedding layer." However, the argument is not persuasive since Reid when considered in combination with Huibers teaches a plurality of such structures formed on a substrate in adjacent fashion such that formation of an array of the suspended structures of Reid results in an array of suspended structures over a space whose endpoints are defined by sidewalls of the embedding layer. Thus, using the process of Reid would necessarily provide a space defined by plural sidewalls under the suspended structure, and an embedding layer surrounding the sacrificial layer an interface being formed between the sidewalls of the sacrificial layer and internal sidewalls of the embedding layer, as recited in the claims, simply by forming a plurality of the structures in adjacent fashion as shown by Huibers

Applicant has argued that after planarization, the sacrificial layer 42 surrounds the plug 44, concluding that Reid fails to disclose "*planarization of the embedding layer such that the front face of the sacrificial layer and a front face of the embedding layer form a common flat surface, the embedding layer still surrounding the sacrificial layer*." However, the argument is not persuasive because Reid when considered in combination with Huibers teaches a plurality of such structures formed on a substrate in adjacent fashion such that formation of an array of the suspended structures of Reid results in an array of suspended structures over a space whose endpoints are defined by sidewalls of the embedding layer. Thus, using the process of Reid to form plural structures would necessarily provide the claim limitations as recited.

Applicant has argued that in Huibers, the attachment regions 54 do not surround the sacrificial material, even if several are manufactured on a single substrate. However, the argument is not persuasive, because the argument considers only Huibers alone, and one cannot show nonobviousness

by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8, 9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent Application Publication 2002/0047172 to Reid in view of U.S. Patent 5,835,256 to Huibers, and WO 00/33089 A2 to Matheiu et al. and in further view of U.S. Patent 5,985,748 to Watts and U.S. Patent 6,090,712 to Lyons.

Regarding Claim 8, Reid teaches a production process of an integrated micro-system type component, (Figures 2A-2G and Paragraphs 19-24) comprising a flat suspended micro-structure, arranged on an embedding layer, the process successively comprising: deposition of a sacrificial layer on a substrate, deposition on at least part of the substrate and on at least part of the front face of the sacrificial layer, of the embedding layer presenting a larger thickness than the thickness of the sacrificial

layer, planarization of the embedding layer such that the front face of the sacrificial layer and a front face of the embedding layer form a common flat surface, deposition of a formation layer (46) of the suspended structure on a front face of the common flat surface, patterning at least one opening in the formation layer up to the level of the front face of the sacrificial layer, and etching the sacrificial layer through the opening such that the suspended structure is suspended over a space having an endpoint defined by a sidewall of the embedding layer.

Reid does not expressly teach that the patterning the opening in the formation layer comprises etching. However, since etching is conventional for patterning the deposited layer, it would have been an immediately envisaged by one of ordinary skill in the art for patterning the deposited layer, although not expressly recited.

Reid does not expressly teach plural sidewalls defining the space under the suspended structure an interface being formed between the sidewalls of the sacrificial layer and internal sidewalls of the embedding layer. However, as taught by Reid, forming an array of adjacent suspended micro-devices such as micro-mirrors is conventional in the art of forming such devices. Although only one suspended structure is shown for illustration, Reid teaches it is conventional to form adjacent suspended microstructures in an array. (See Col. 1, Lines 15-33 and Col. 4, Lines 36-41) For example, Huibers, is incorporated by reference, and teaches a micro-mirror array (Figures 1-8) having immediately adjacent suspended structures. It would have been obvious to one of ordinary skill in the art at the time of invention to form the microstructure of Reid in an array in the conventional manner (i.e. by simply repeating the structure in adjacent fashion). The resulting array of suspended structures produced using the process of Reid would necessarily provide a space defined by plural sidewalls under the suspended structure, an interface being formed between the sidewalls of the sacrificial layer and internal sidewalls of the embedding layer, and an embedding layer surrounding the sacrificial layer, as recited and illustrated by applicant.

Reid does not expressly teach that a polymer sacrificial layer is dry etched, however, Reid teaches dry etching techniques for the sacrificial layer (Paragraph 23) and photoresist type sacrificial layers (Paragraph 19), and dry etching such as oxygen plasma, is old and well known in the

microfabrication art for removing photoresist sacrificial layers as shown by Matheiu et al. (Page 23, Lines 20-30) Thus, it would have been obvious to use dry etching on a polymer material such as photoresist.

Regarding Claims 8 and 9, Reid teaches the planarization step comprises chemical mechanical polishing, (Paragraph 23) but does not expressly teach the planarization step successively comprises a chemical mechanical polishing sub-step and an etching sub-step. However, it is old and well known in the chemical mechanical planarizing art to successively use a polishing sub-step and an etching sub-step, in order to prevent over polishing one of the materials resulting in a dishing effect. For example, Watts et al. teaches reducing or eliminating abrasive in the final step.(See Abstract, Fig. 1-4, Col. 2-6) Lyons similarly teaches (Col. 5, Lines 33-55) a first planarization step and a second etching step to provide a planar surface using chemical mechanical polishing. It would have been obvious to one of ordinary skill in the art at the time of invention to perform an etching sub-step in order to provide a highly planarized surface between dissimilar materials without excessive deviation as shown by Watts et al. and Lyons et al.

Regarding Claim 8, Reid teaches the planarization step successively comprise a chemical mechanical polishing sub-step of the embedding layer and an etching sub-step of the embedding layer so that the front faces of the sacrificial layer and of the embedding layer form a common flat surface.

Regarding Claims 11 and 12, Reid teaches the side walls of the sacrificial layer are confined by etching by means of a mask formed on the front face of a layer made from polymer material by deposition, lithography and etching of a temporary layer, deposition of the embedding layer being performed on the assembly formed by the sacrificial layer and the mask, but does not expressly teach that the mask is eliminated in the course of the planarization step or that the planarization step comprises an etching step of the mask. However, since Reid teaches patterning the sacrificial layer (Paragraph 23) and teaches that the photoresist mask for patterning is removed in the well known manner, (Paragraph 19) it would have been obvious to one of ordinary skill in the art at the time of invention to eliminate the mask during the planarization step (which comprises an etching step) since this step removes material down to the sacrificial layer thus eliminating a separate removal step for the photoresist mask.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent Application Publication 2002/0047172 to Reid in view of U.S. Patent 5,835,256 to Huibers, and WO 00/33089 A2 to Matheiu et al. and in further view of U.S. Patent Application Publication 2003/0183887 to Lee et al.

Regarding Claim 13, Reid teaches a production process of an integrated micro-system type component, (Figures 2A-2G and Paragraphs 19-24) comprising a flat suspended micro-structure, arranged on an embedding layer, the process successively comprising: deposition of a sacrificial layer on a substrate, deposition on at least part of the substrate and on at least part of the front face of the sacrificial layer, of the embedding layer presenting a larger thickness than the thickness of the sacrificial layer, planarization of the embedding layer such that the front face of the sacrificial layer and a front face of the embedding layer form a common flat surface, deposition of a formation layer (46) of the suspended structure on a front face of the common flat surface, patterning at least one opening in the formation layer up to the level of the front face of the sacrificial layer, and etching the sacrificial layer through the opening such that the suspended structure is suspended over a space having an endpoint defined by a sidewall of the embedding layer.

Reid does not expressly teach that the patterning the opening in the formation layer comprises etching. However, since etching is conventional for patterning the deposited layer, it would have been an immediately envisaged by one of ordinary skill in the art for patterning the deposited layer, although not expressly recited.

Reid does not expressly teach plural sidewalls defining the space under the suspended structure. However, as taught by Reid, forming an array of adjacent suspended micro-devices such as micro-mirrors is conventional in the art of forming such devices. Although only one suspended structure is shown for illustration, Reid teaches it is conventional to form adjacent suspended microstructures in an array. (See Col. 1, Lines 15-33 and Col. 4, Lines 36-41) For example, Huibers, is incorporated by reference, and teaches a micro-mirror array (Figures 1-8) having immediately adjacent suspended structures. It would have been obvious to one of ordinary skill in the art at the time of invention to form the microstructure of Reid in an array in the conventional manner (i.e. by simply repeating the structure in adjacent fashion).

The resulting array of suspended structures produced using the process of Reid would necessarily provide a space defined by plural sidewalls under the suspended structure as recited and illustrated by applicant.

Reid does not expressly teach that a polymer sacrificial layer is dry etched, however, Reid teaches dry etching techniques for the sacrificial layer (Paragraph 23) and photoresist type sacrificial layers (Paragraph 19), and dry etching such as oxygen plasma, is old and well known in the microfabrication art for removing photoresist sacrificial layers as shown by Matheiu et al. (Page 23, Lines 20-30) Thus, it would have been obvious to use dry etching on a polymer material such as photoresist.

Regarding Claim 13, Reid does not expressly teach additionally forming salient (projecting prominent, conspicuous) elements. However, Lee et al teach before deposition of a sacrificial layer, deposition on at least one zone of the substrate designed to be covered by the sacrificial layer and comprising salient elements (320, 330, 420, 430), of a base layer (340, 440) presenting a larger thickness than the thickness of the salient elements, and an additional planarization step, by chemical mechanical polishing, of the base layer (Figure 3D, 4D) so that the front face of the base layer and of the salient elements form a common flat surface.

It would have been obvious to one of ordinary skill in the art at the time of invention to form the sacrificial layer over planarized salient elements as shown by Lee et al. in order to provide a driving electrode for a micromechanical device.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberts P. Culbert whose telephone number is (571) 272-1433. The examiner can normally be reached on Monday-Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberts P Culbert/
Primary Examiner, Art Unit 1792